

## Revision:3.01

www.xinxunwei.com 400-800-9990

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05	PROCESSOR DDRIII INTERFACE
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11	MCP61-PCI_EXPRESS
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[illegible]

<b>GIGABYTE</b>				
Title				
<b>BLOCK DIAGRAM</b>				
Size	Document Number			Rev
Custom	<b>GA-M52LT-D3P</b>			<b>3.0</b>
Date:	Wednesday, December 29, 2010		Sheet	1 of 30

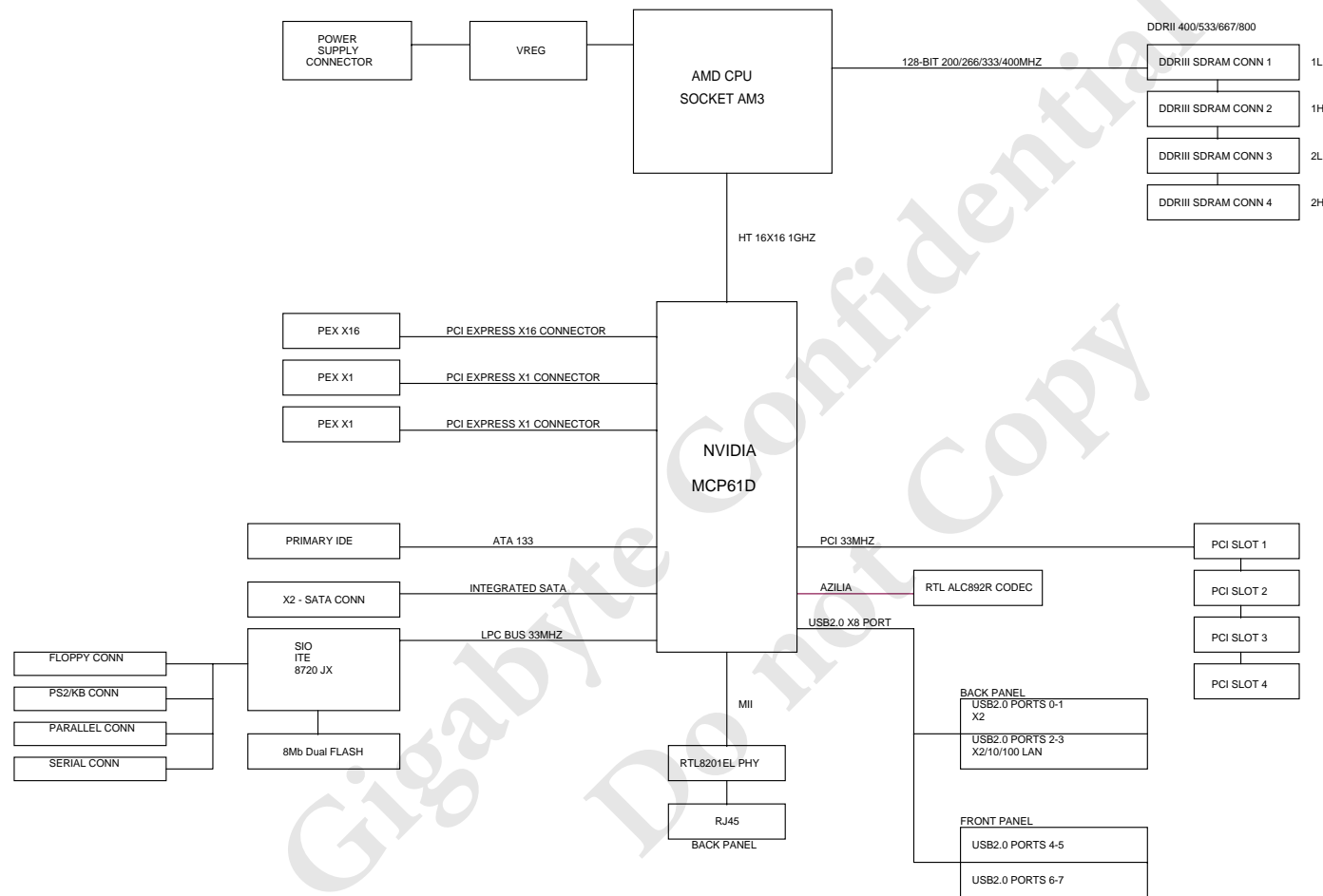
**P-Code: U96058-0**

[illegible]

## Reason

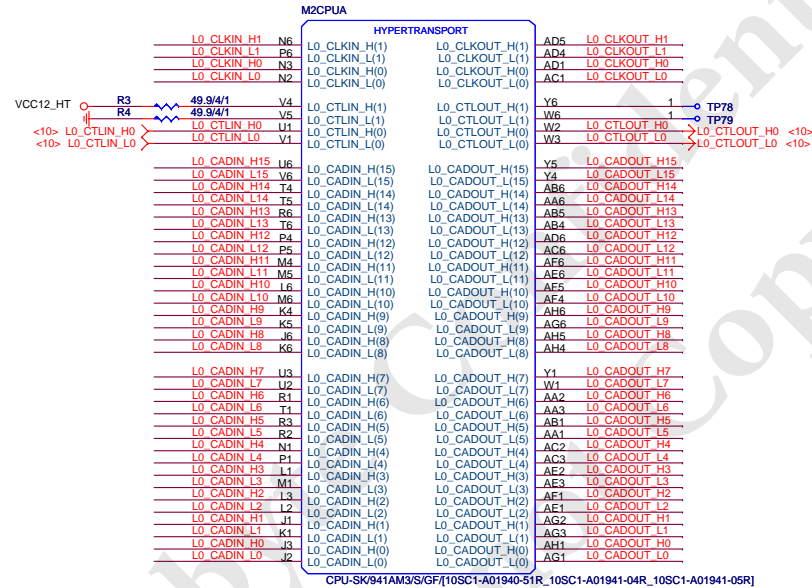
[illegible]

## BLOCK DIAGRAM

**GIGABYTE**

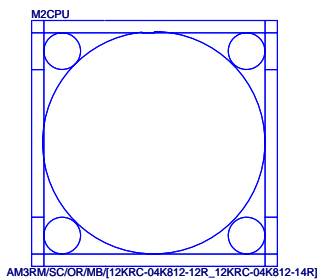
Title			
BLOCK DIAGRAM			
Size	Document Number	Rev	
Custom	GA-M52LT-D3P	3.01	
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L0\_CADIN\_L[0..15] <L0\_CADIN\_L[0..15] <10>  
 L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] <10>  
 L0\_CLKIN\_L[0..1] <L0\_CLKIN\_L[0..1] <10>  
 L0\_CLKIN\_H[0..1] <L0\_CLKIN\_H[0..1] <10>  
 L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] <10>  
 L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] <10>  
 L0\_CLKOUT\_L[0..1] <L0\_CLKOUT\_L[0..1] <10>  
 L0\_CLKOUT\_H[0..1] <L0\_CLKOUT\_H[0..1] <10>



CPU\_VDD\_RUN = VCORE  
 CPU\_VDDA\_RUN = VDDA25  
 VLDT\_RUN = VCC12\_HT  
 CPU\_VDDIO\_SUS = DDR18V  
 CPU\_VTT\_SUS = DDRVTT

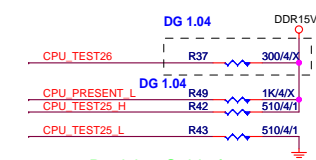
VLDT\_A = VCC12\_HT  
 VLDT\_B = HT12B



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Title			
CPU HYPER TRANSPORT			
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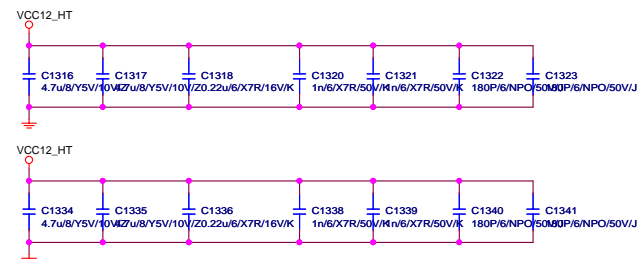
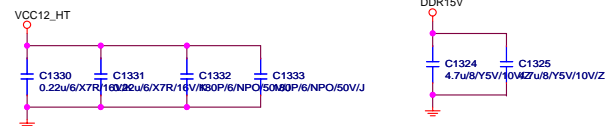
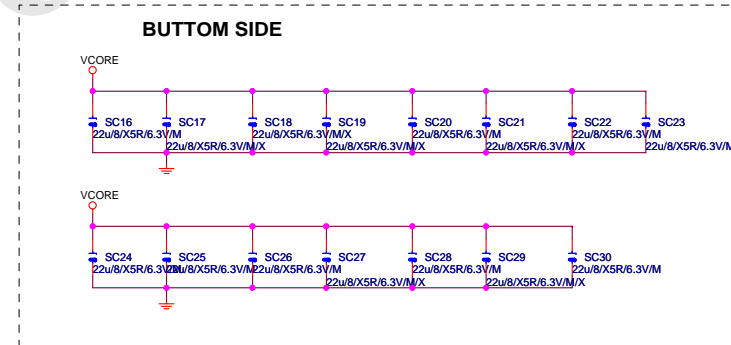
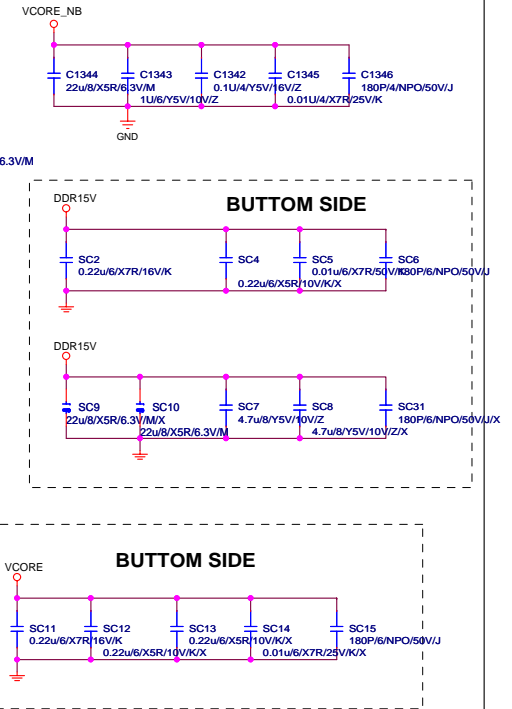




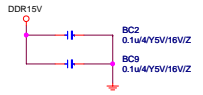
CPU-SK/941AM3/S/GF/[10SC1-A01940-51R\_10SC1-A01941-04R\_10SC1-A01941-05R]



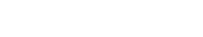
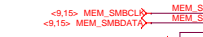
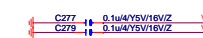
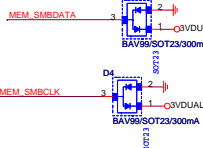
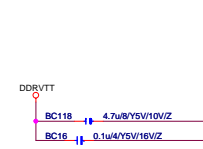
VLDT\_RUN\_B is connected to the VLDT\_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



## DDR15V Decouple



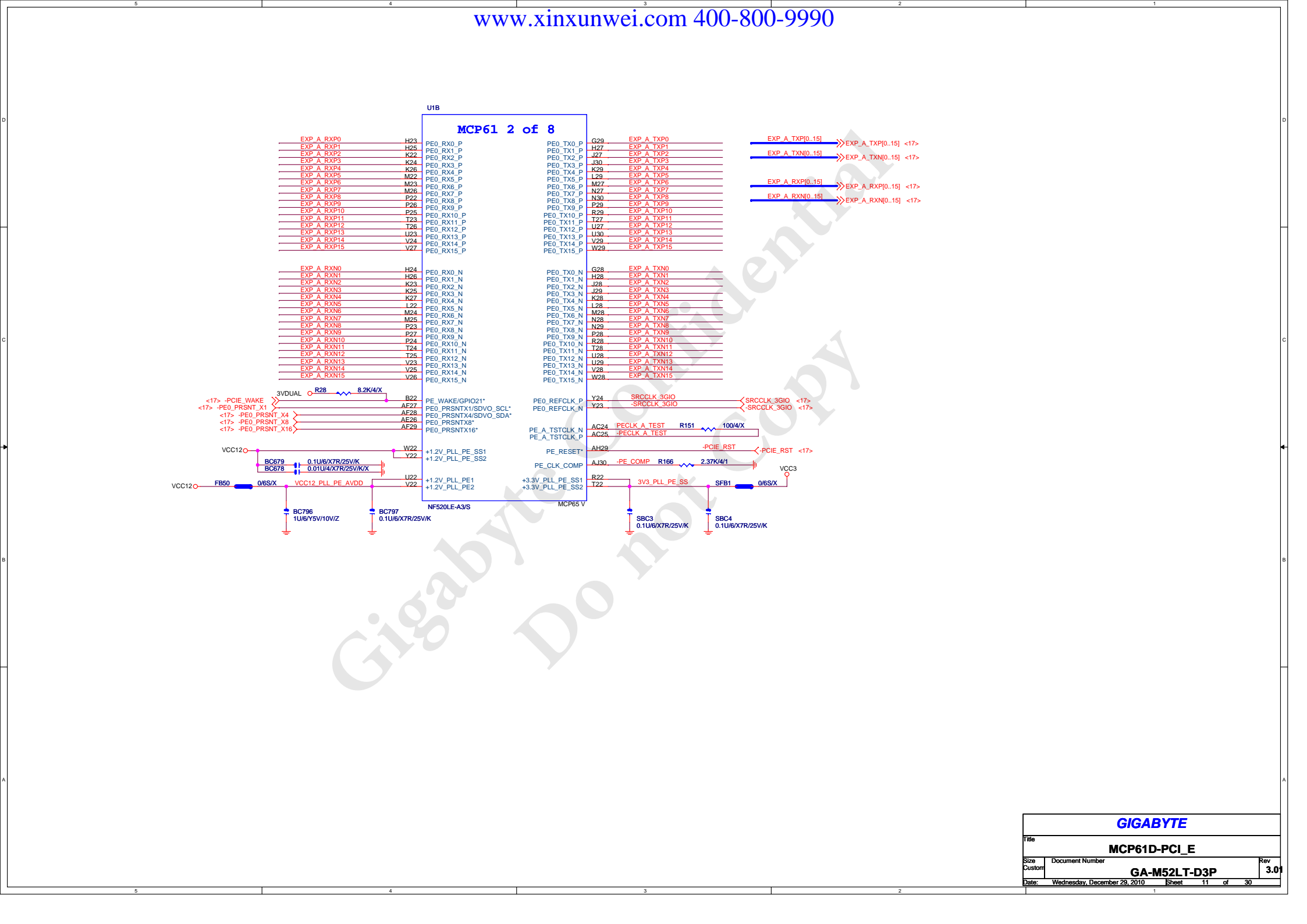
## DDRVTT Decouple

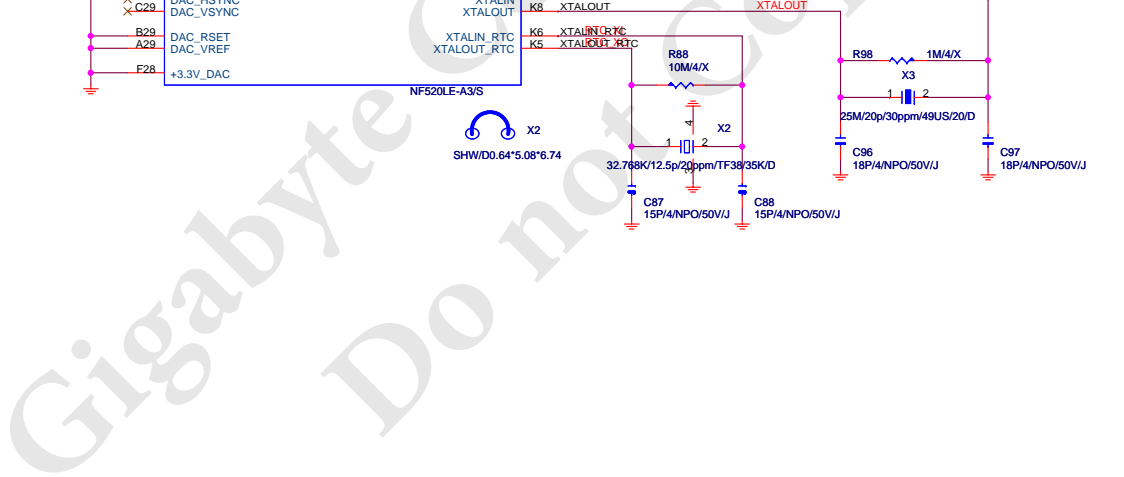


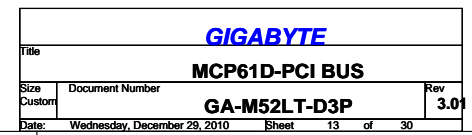
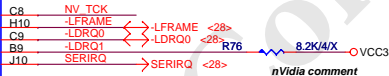
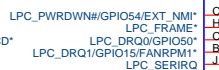
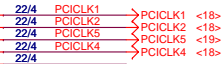
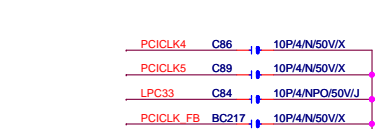


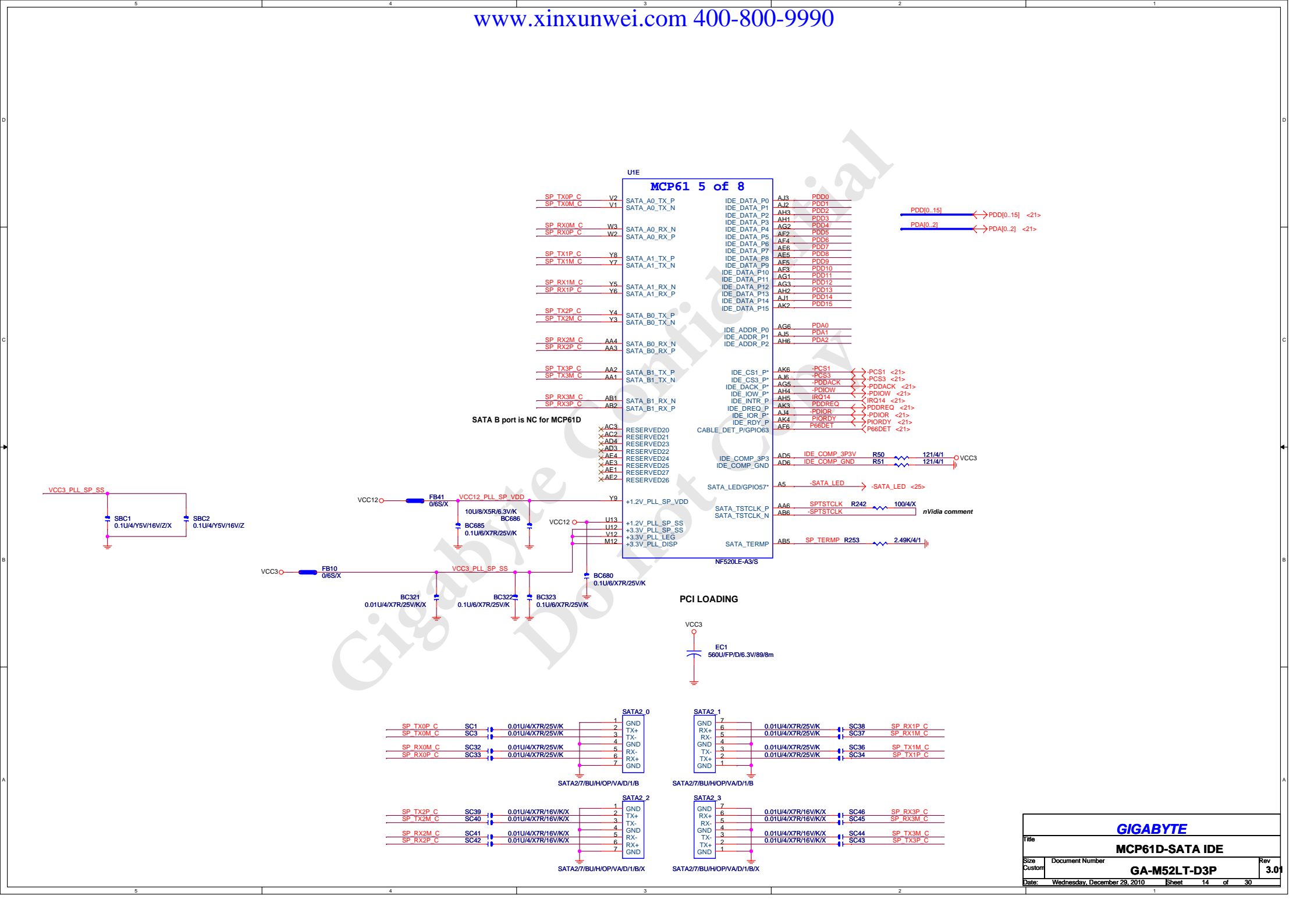


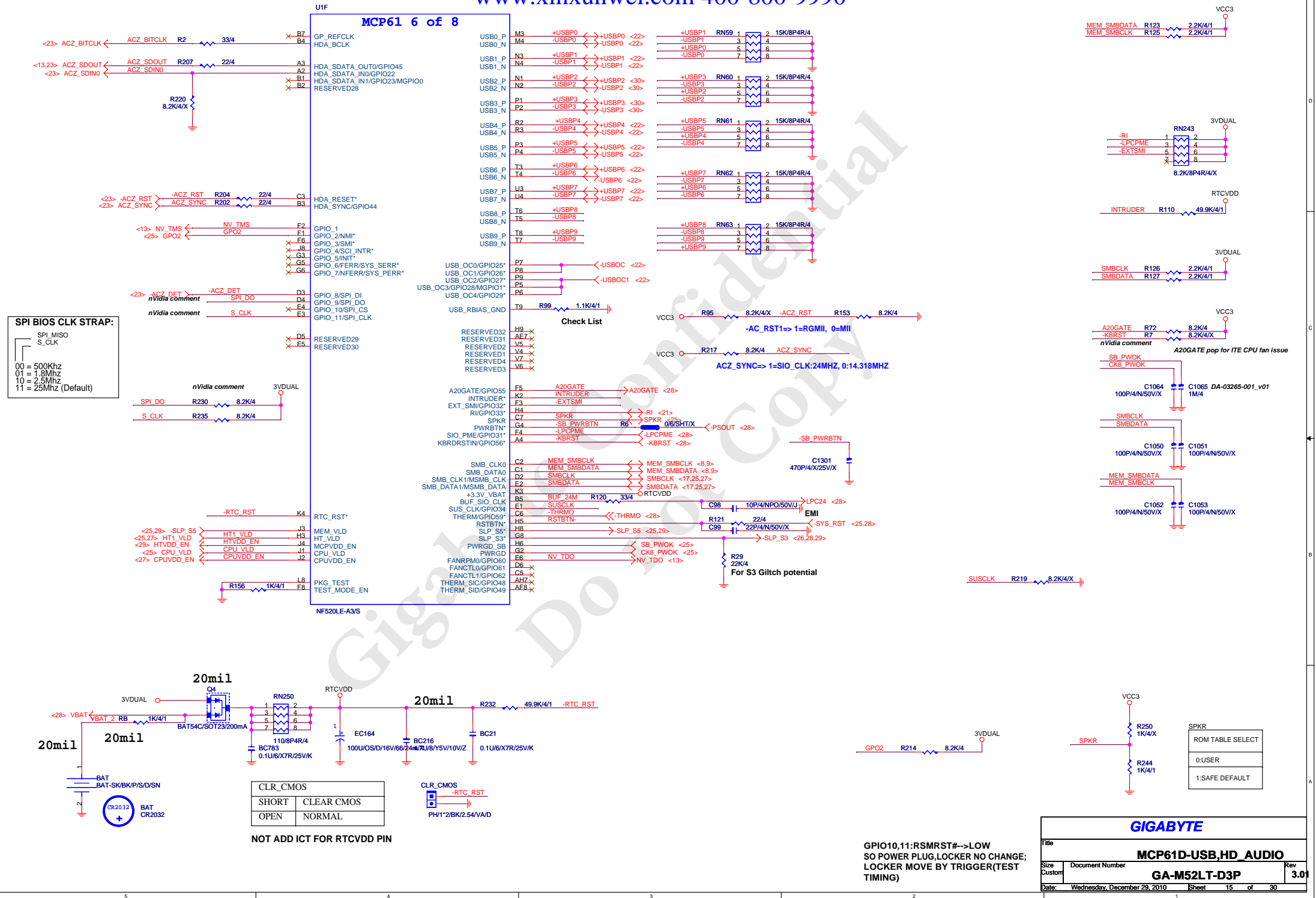


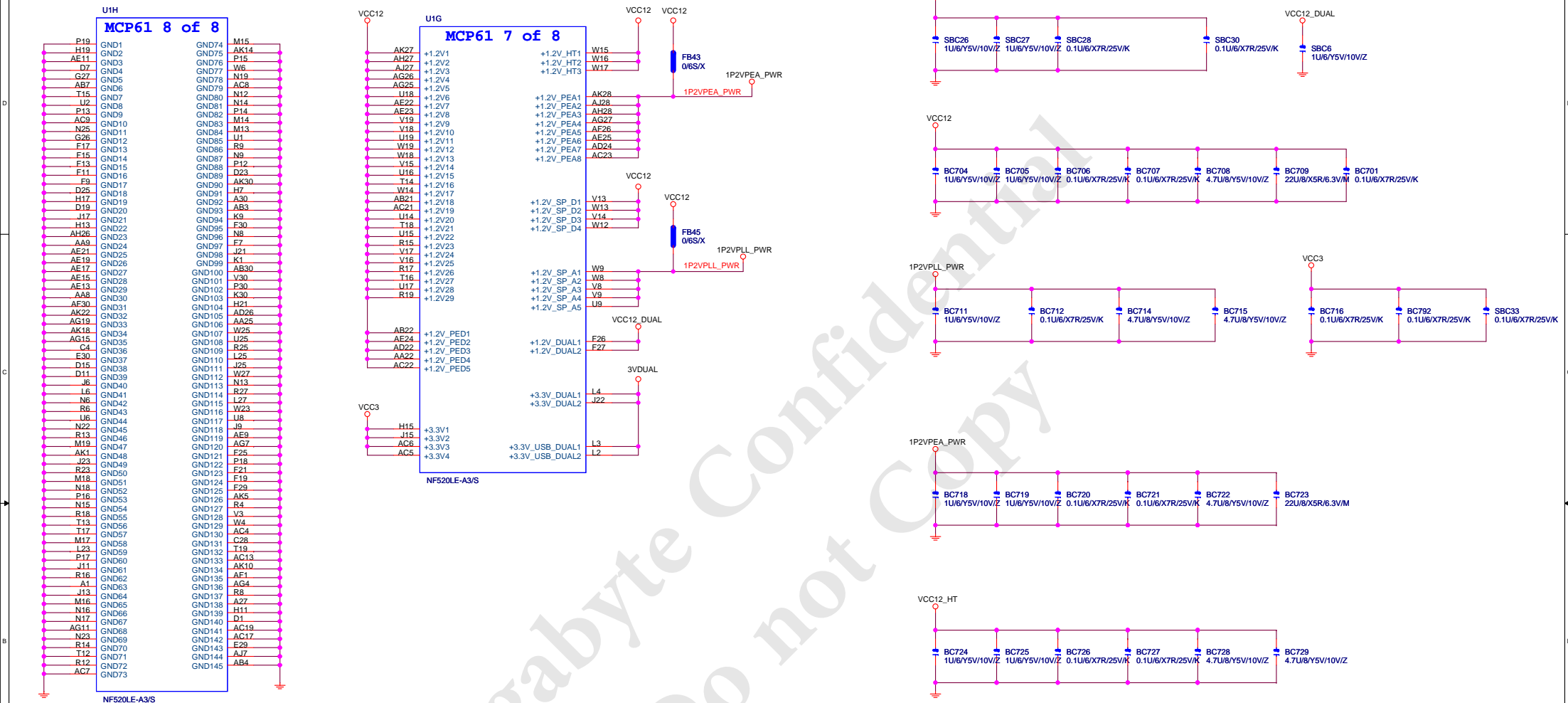




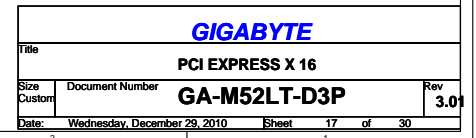


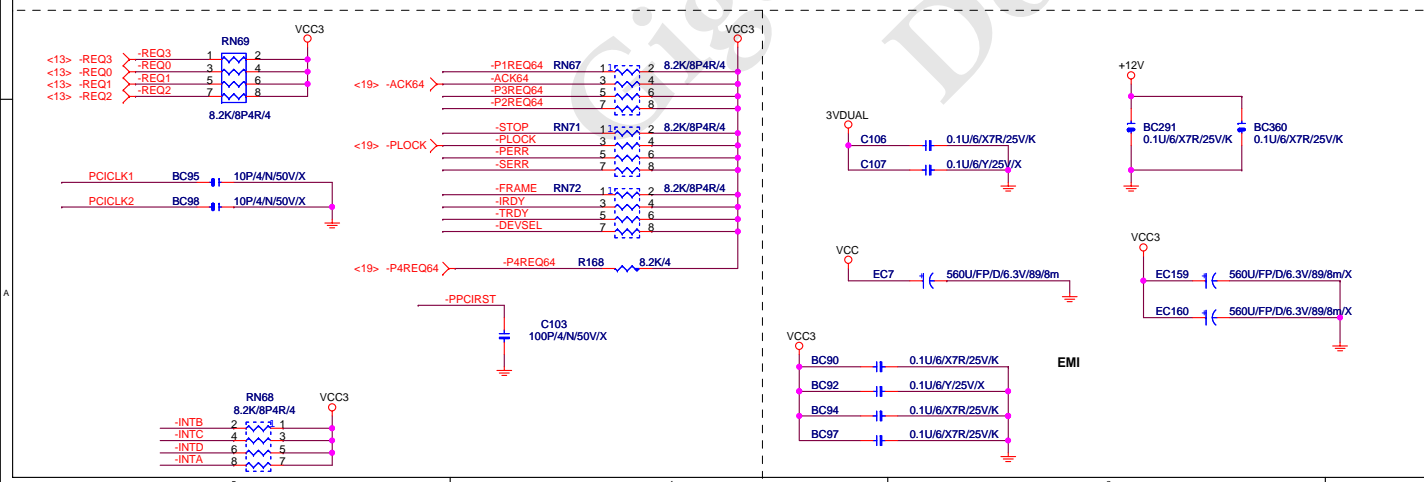
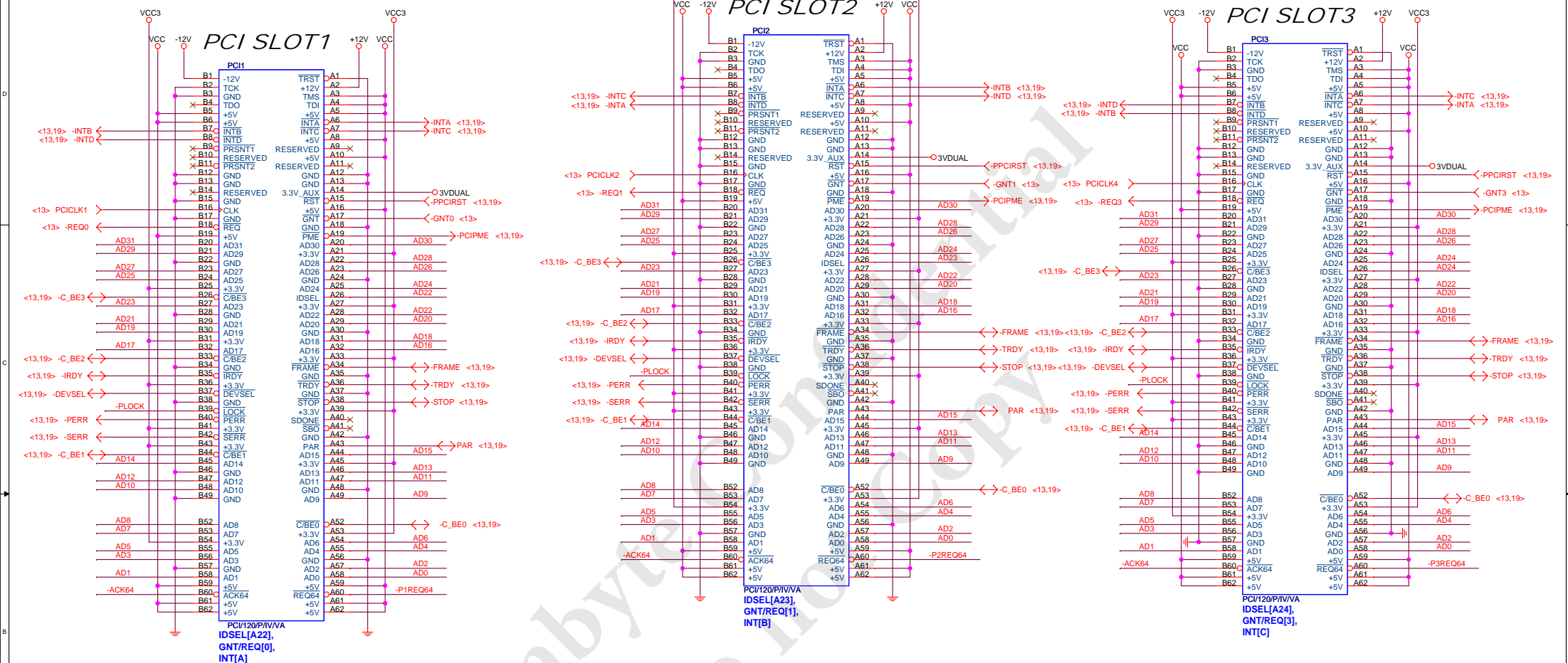


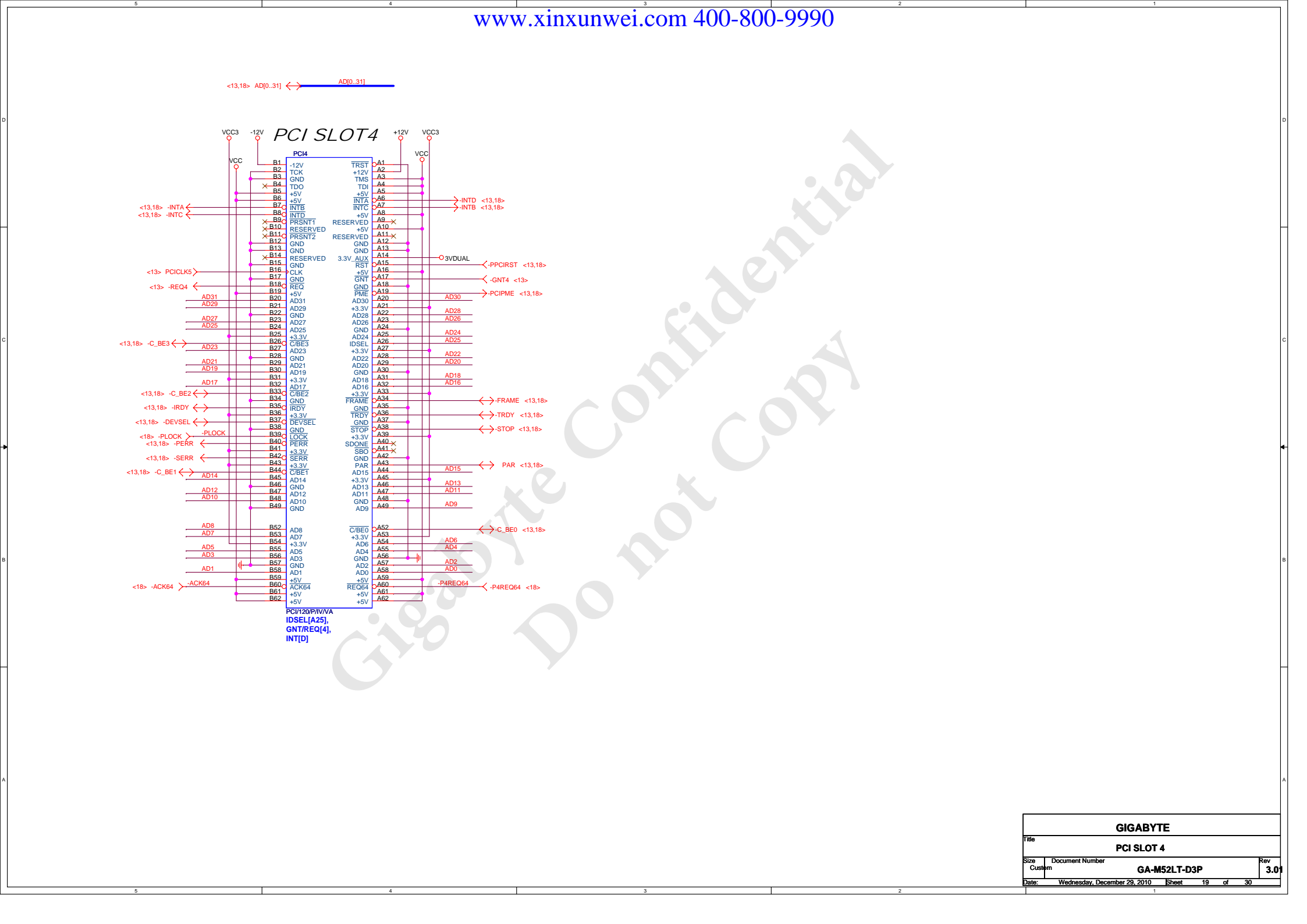




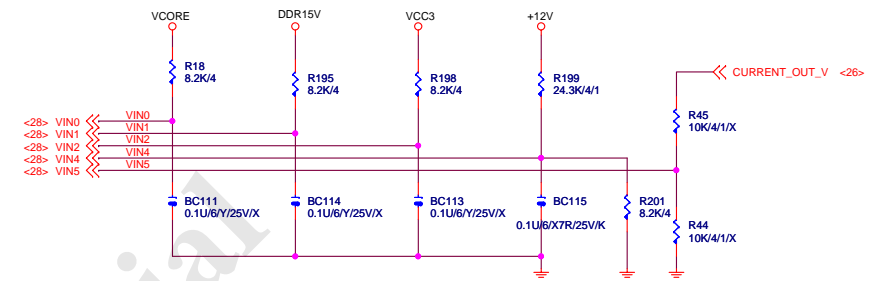
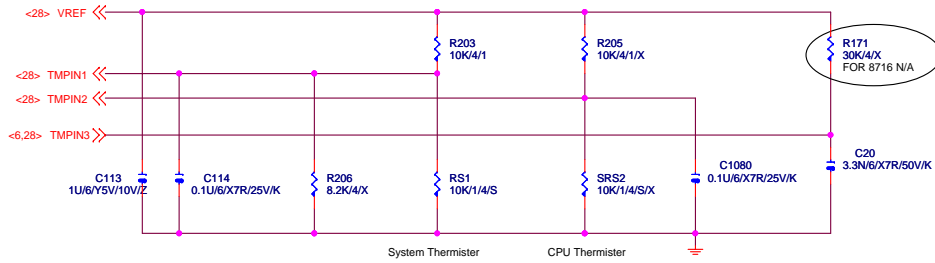




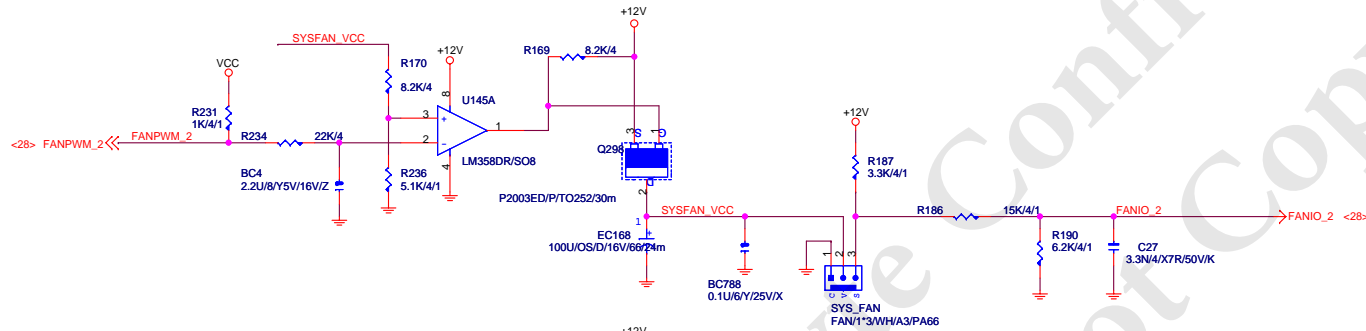




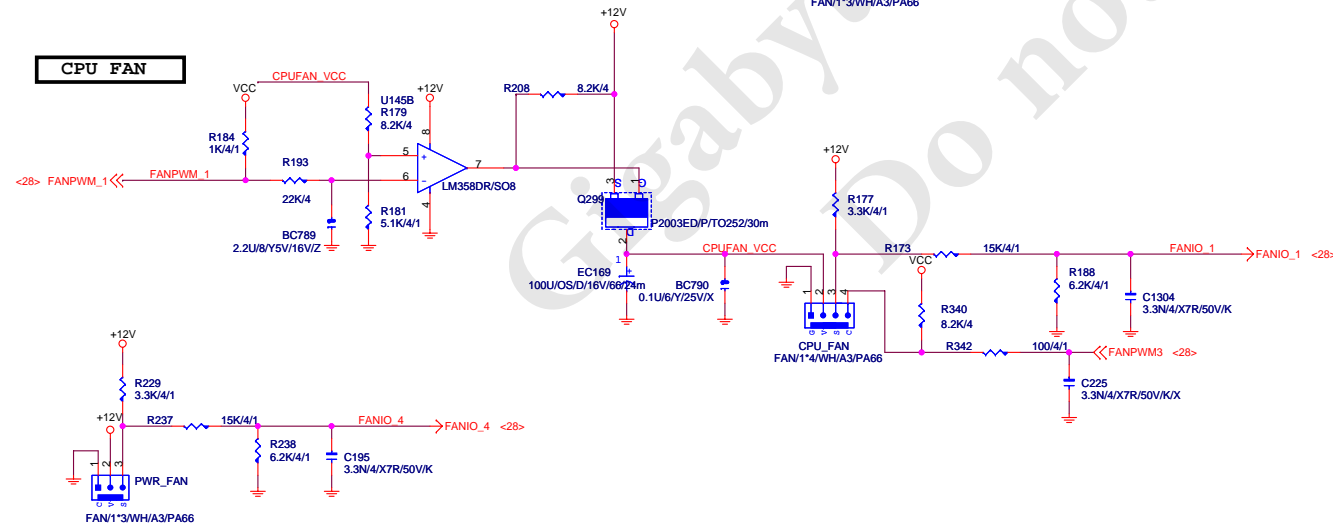
## Hardware Monitor circuits



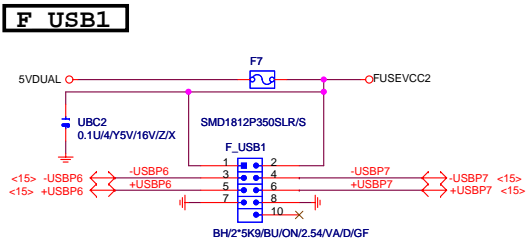
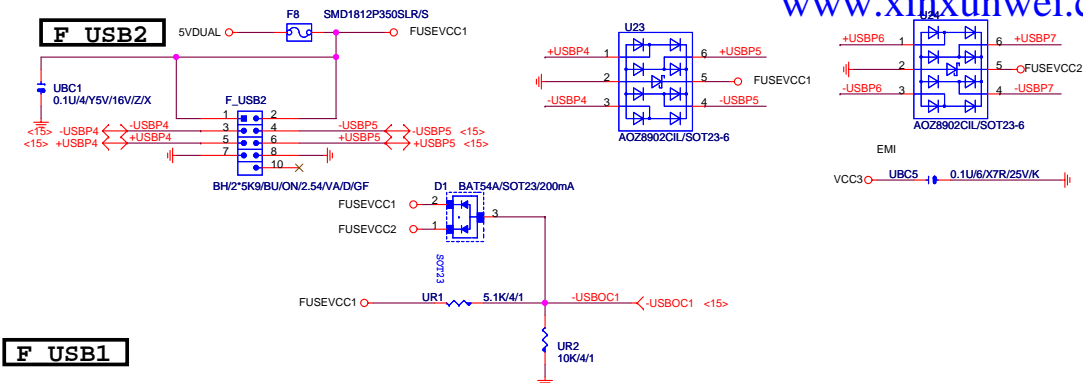
## SYSTEM FAN



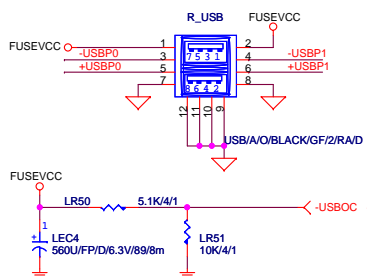
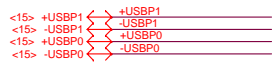
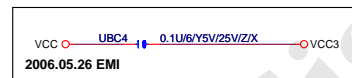
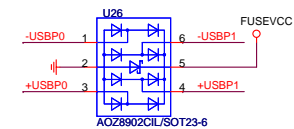
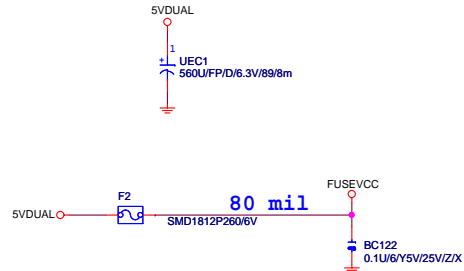
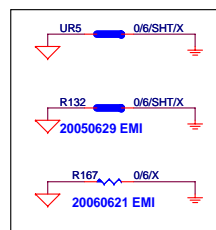
## CPU FAN





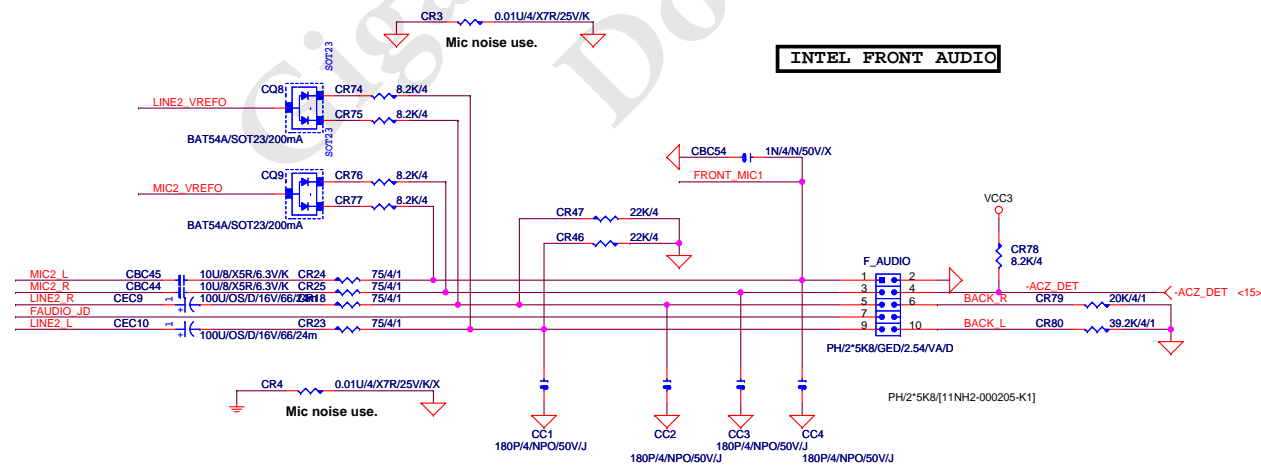
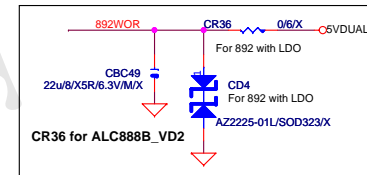
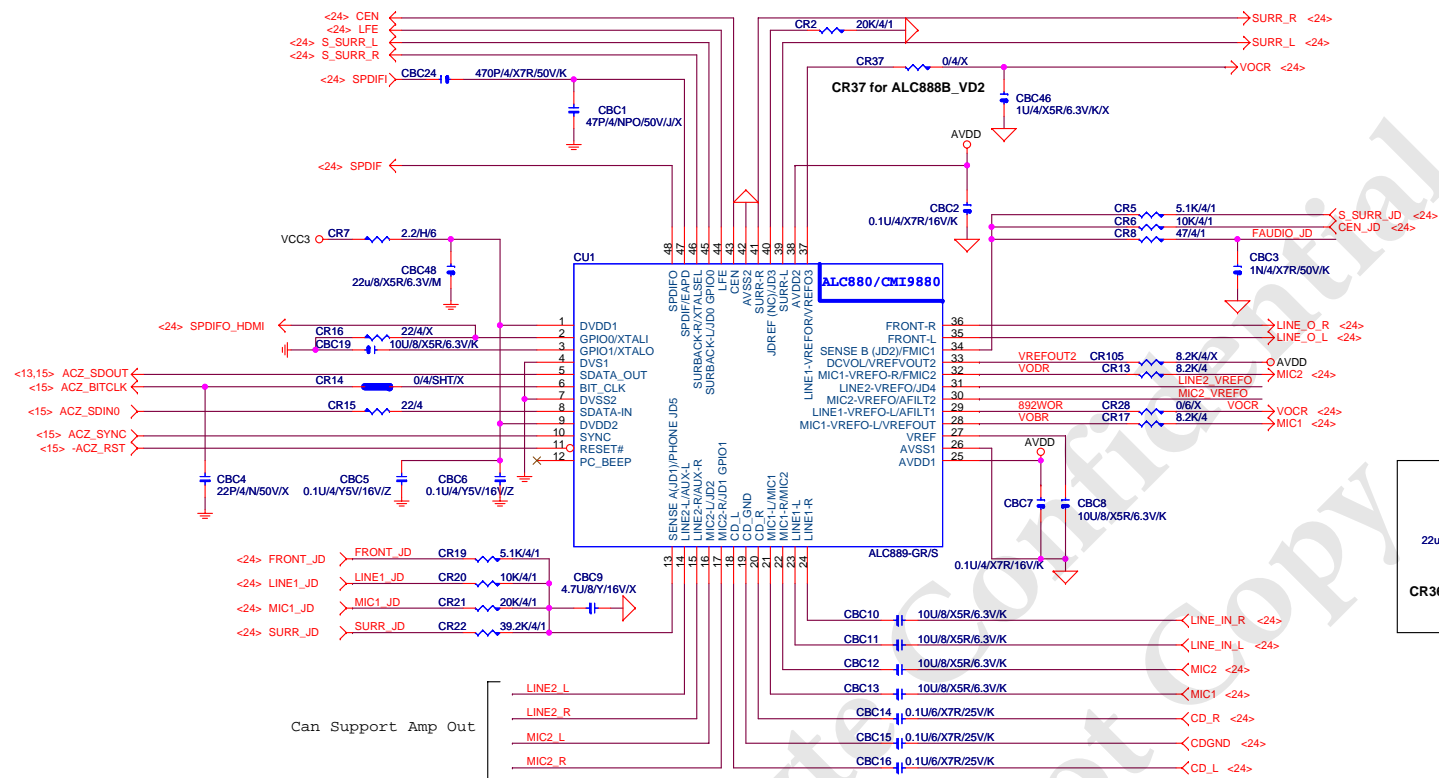


1012 EMI



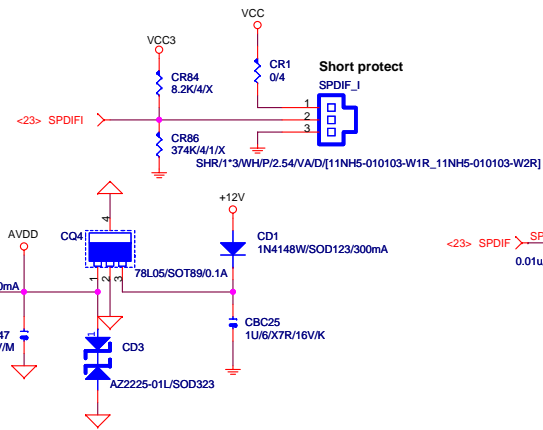
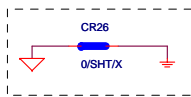
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USB PORT			
Size	Document Number	Rev	
Custom	GA-M52LT-D3P	3.01	
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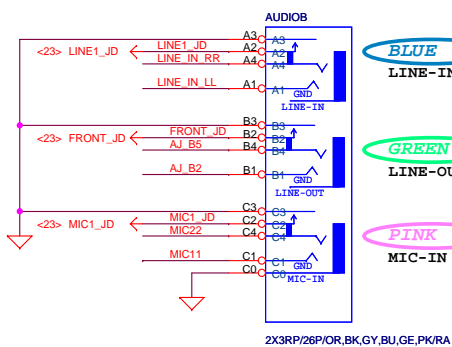
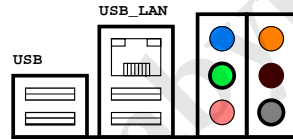
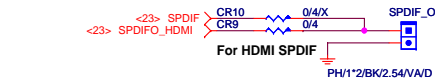
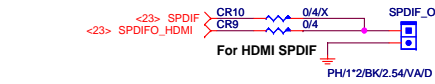
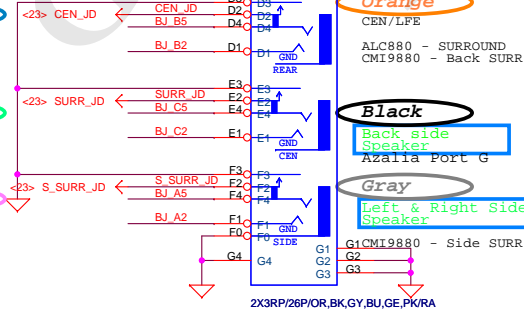
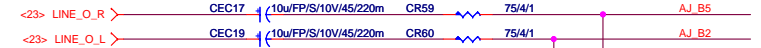


GIGABYTE

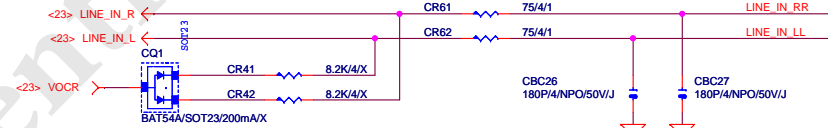
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Size	Document Number	GA-M52LT-D3P	
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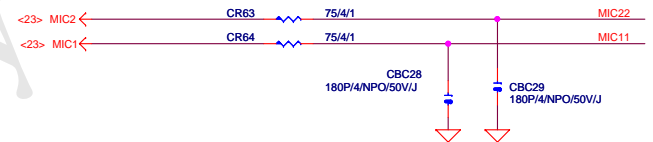
## CD IN

BLUE  
LINE-INGREEN  
LINE-OUTPINK  
MIC-INOrange  
CEN / LFE  
ALC880 - SURROUND  
CMI9880 - Back SURRBlack  
Back side  
Speaker  
Azalia Port GGray  
Left & Right Side  
SpeakerG1 CMI9880 - Side SURR  
G2  
G3A3RJ/13P/B[11NR6-403006-01\_11NR6-403006-02]  
3RJ+15F[11NR6-403004-11]A3RJ/13P/OBG[11NR6-403006-71]  
3RJ+15F[11NR6-403004-31]LINE OUT  
FRONT OUT

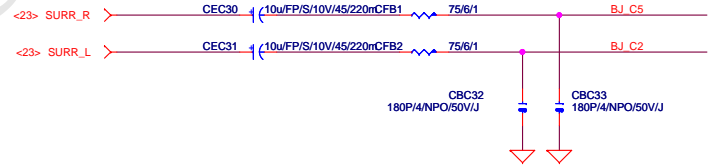
## LINE-IN



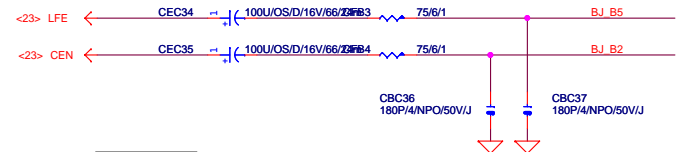
## MIC



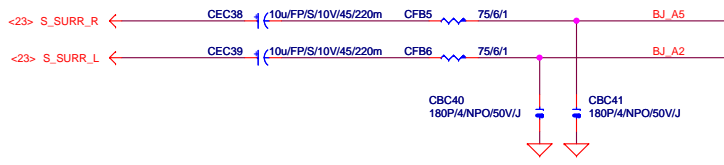
## SURROUND



## CEN/LFE



## SURR BACK



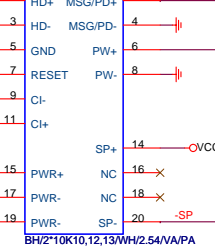
GIGABYTE

Title		
AUDIO JACK		
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# INTEL FRONT PANEL

F. PANEL



BH/2\*10K10,12,13/WH/2.54/A/PA

VCC

D20 1N4148W/SOD123/300mA

R455 75/6/1 R456 75/6/1 Q98 2N7002/SOT23/25PF/5

R460 1K/4/1 Q108 MMBT2222A/SOT23/600mA/40

R461 8.2K/4 Q107 MMBT2222A/SOT23/600mA/40

R470 1K/4/1

MMBT2222A/SOT23/600mA/40

3VDUAL R212 8.2K/4

HT1\_VLD <15,27>

5VSB C162 0.1u/6/Y/25V/X

Q279 2N7002/SOT23/25PF/5

R343 8.2K/4

Q58 MMBT2222A/SOT23/600mA/40

SOT23

VCC12\_HT R346 6.2K/4/1

C163 0.33u/6/Y/16V/Z

3VDUAL

R335 15K/4/1

SB\_PWOK <15>

5VSB R334 8.2K/4

Q54 2N7002/SOT23/25PF/5

C152 1u/6/Y/16V/Z/X

Q53 2N7002/SOT23/25PF/5

3VDUAL R31 15K/4/1

C154 4.7u/8/Y/10V/Z

For plug, unplug quickly. Make sure SB\_PWOK is rising from Zero.

<15,28> -SYS\_RST

<28> DBIOS\_RST

3VDUAL R444 8.2K/4/X

R447 33/4/X

RESET

C199 0.01u/4/Y/10V/X

Q1 BAV99/SOT23/300mA

5VSB

3VDUAL R94 1K/4/1/X

Q8 MMBT2222A/SOT23/600mA/40/X

SOT23

3VDUAL R10 8.2K/4/X

R106 1K/4/1/X

<28> DBIOS\_RST

RESET

3VDUAL

Q8 MMBT2222A/SOT23/600mA/40/X

SOT23

3VDUAL

Q8 MMBT2222A/SOT23/600mA/40/X

SOT23

3VDUAL

Q8 MMBT2222A/SOT23/600mA/40/X

SOT23

3VDUAL

Q8 MMBT2222A/SOT23/600mA/40/X

SOT23

3VDUAL

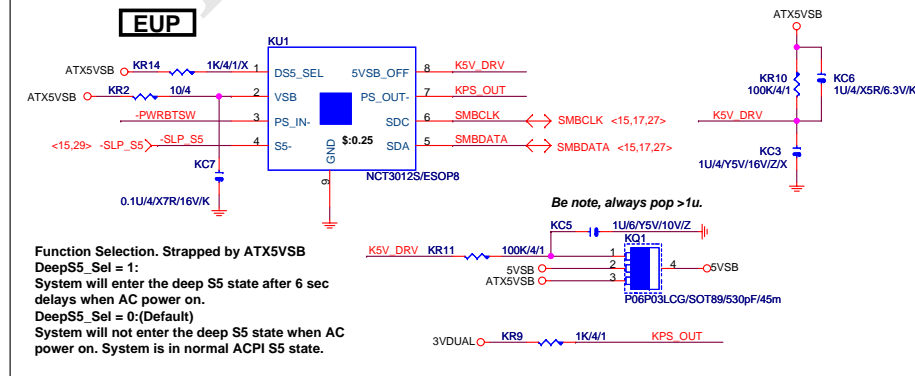
Q8 MMBT2222A/SOT23/600mA/40/X

SOT23

3VDUAL

Q8 MMBT2222A/SOT23/600mA/40/X

SOT23



<14> -SATA\_LED -SATA\_LED

<21> -IDEACTP -IDEACTP

D2 BAT54A/SOT23/200mA

C112 180P/4/N/50V/X

<27> VCORE\_PWOK

R352 8.2K/4

5VSB

R339 8.2K/4

Q3 2N7002/SOT23/25PF/5

CPU\_VLD <15>

VCC3

R338 8.2K/4

Q3 2N7002/SOT23/25PF/5

CPU\_VLD <15>

5VSB

R337 8.2K/4

Q55 2N7002/SOT23/25PF/5

CK8\_PWOK <15>

3VDUAL

R336 8.2K/4

Q56 2N7002/SOT23/25PF/5

C1302 0.1u/6/Y/25V/X

5VSB

R337 8.2K/4

Q55 2N7002/SOT23/25PF/5

CK8\_PWOK <15>

3VDUAL

R336 8.2K/4

Q56 2N7002/SOT23/25PF/5

C1302 0.1u/6/Y/25V/X

5VSB

R337 8.2K/4

Q55 2N7002/SOT23/25PF/5

CK8\_PWOK <15>

3VDUAL

R336 8.2K/4

Q56 2N7002/SOT23/25PF/5

C1302 0.1u/6/Y/25V/X

5VSB

R337 8.2K/4

Q55 2N7002/SOT23/25PF/5

CK8\_PWOK <15>

## Control pin

This design MAX 3A

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

R130 1.3K/4/1

R124 1.21K/4/1

C169 1u/4/X/5R/6.3V/K

5VSB

R134 100/4/1

Q19 AP431N/SOT23/150mA

CE4 100u/OS/D/16V/66/24m

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

U17A LM358DR/S08

WR23 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

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HT\_EN2

2.5LEVEL

HT\_EN2

U17B LM358DR/S08

WR25 100/4/1

HT\_EN2

2.5LEVEL

HT\_EN2

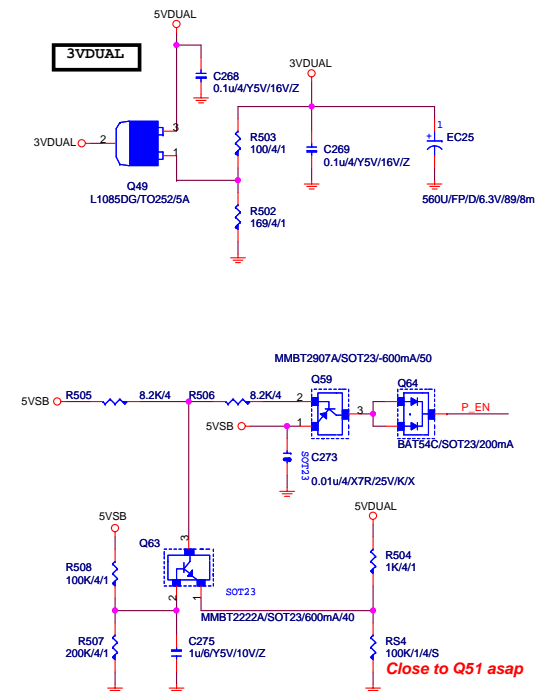
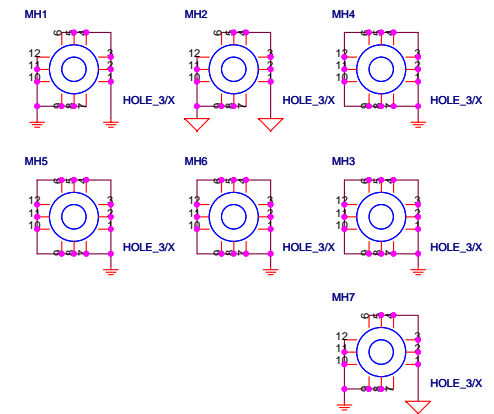
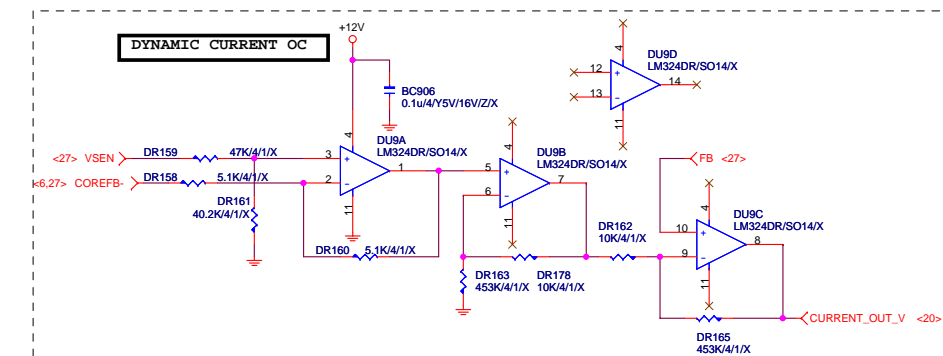
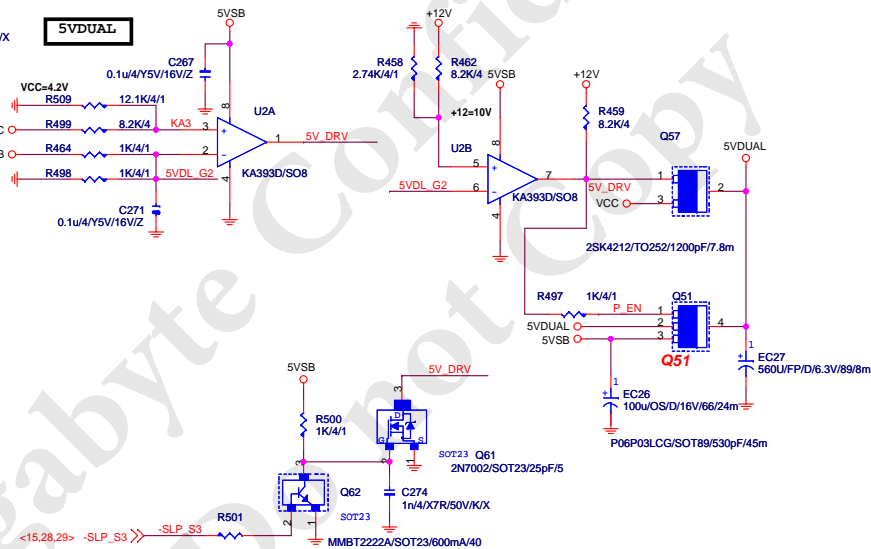
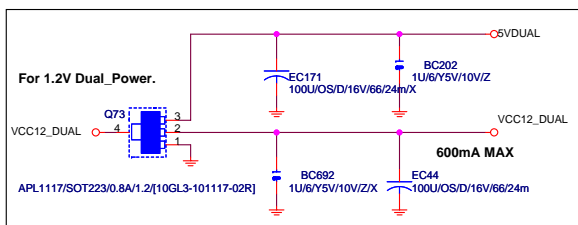
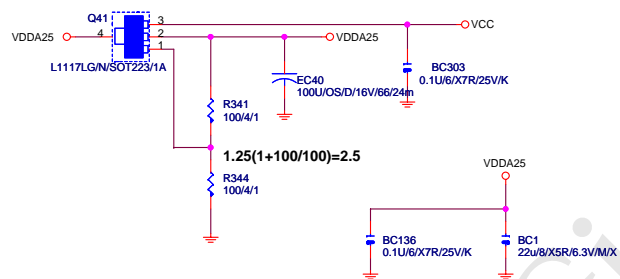
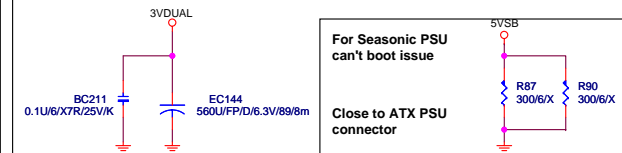
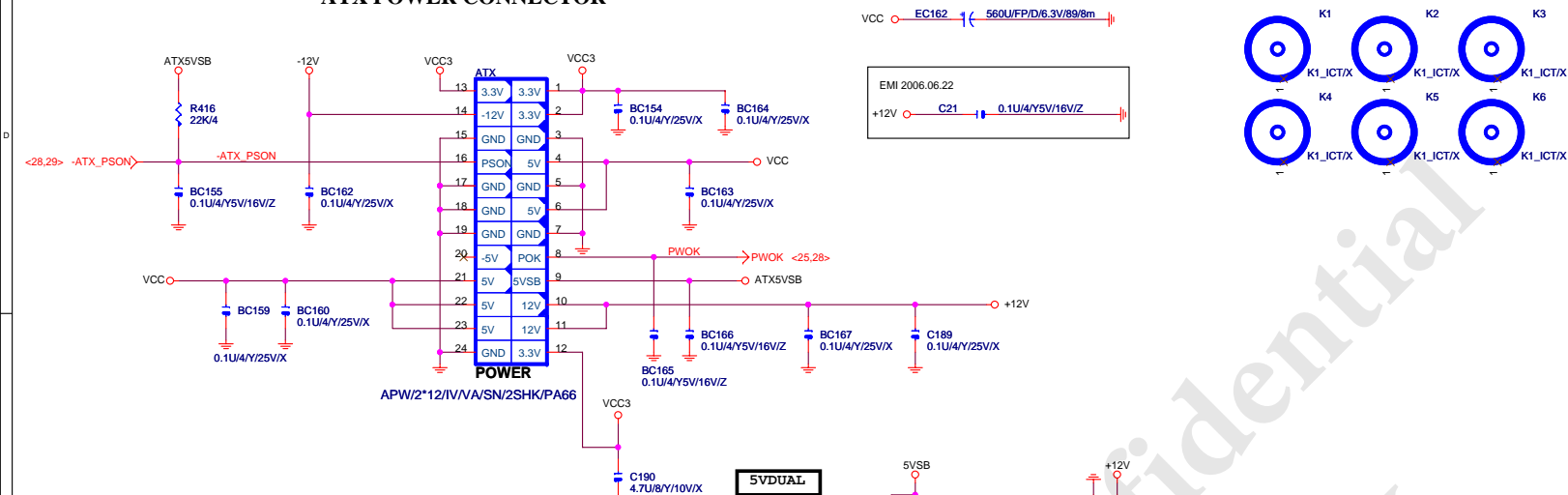
U17A LM358DR/S08

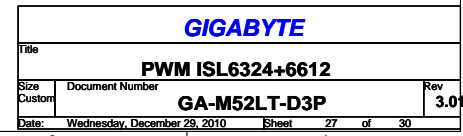
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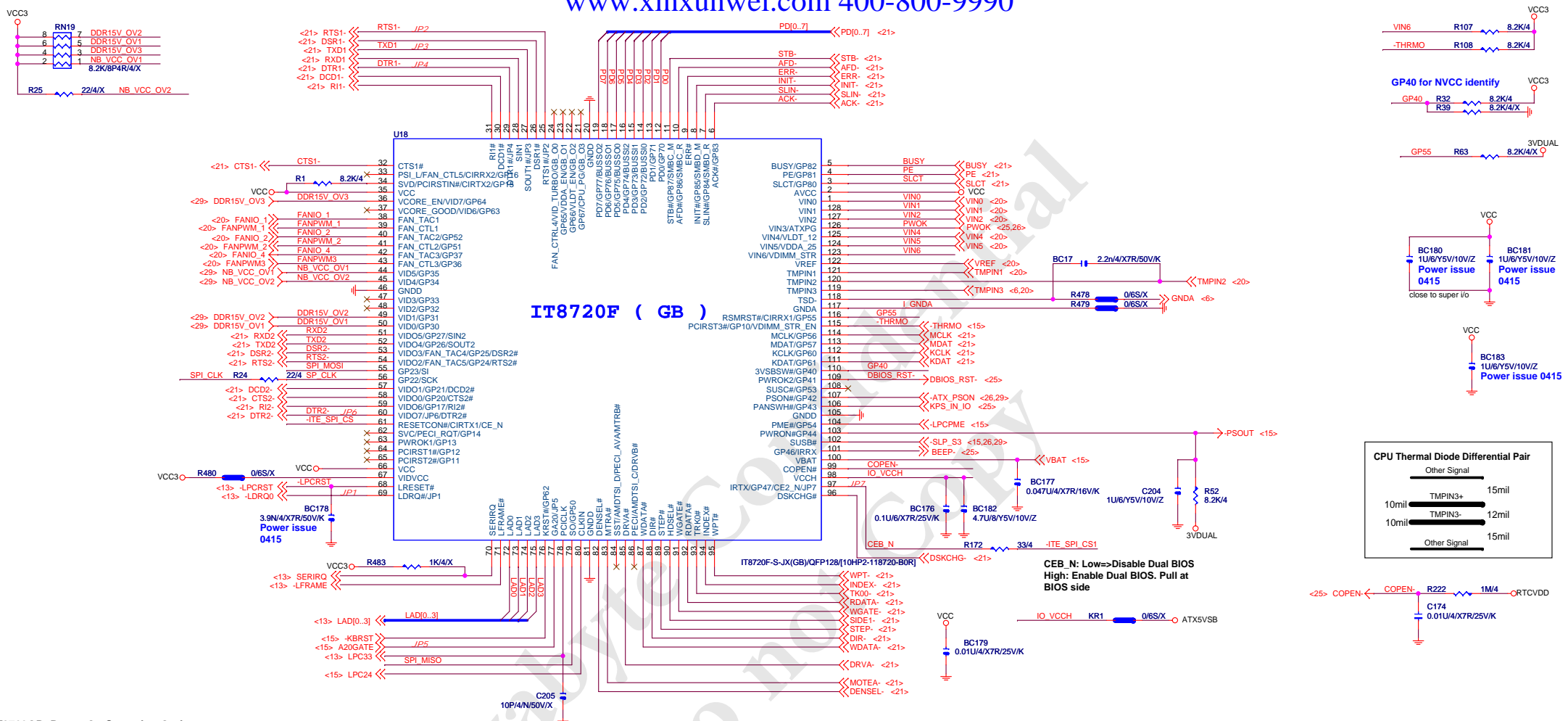
HT\_EN2

2.5LEVEL

## ATX POWER CONNECTOR







IT8720GB Power On Strapping Options

Symbol	value	Description
JP1	Flashseg1_EN	1 Disabled.
Pin 69	Flash I/F Address Segment 1 is enabled	
JP2	VIDO_EN	1 Disable VID output pins
Pin 25	VIDO_EN	0 Enable VID output pins
JP3	CHIP_SEL	Chip selection in Configuration
Pin 27	CHIP_SEL	
JP4	K8PWR_EN	1 K8 power sequence disabled
Pin 29	K8PWR_EN	0 K8 power sequence enabled
JP3 & JP5	FAN_CTL_SEL	11 Half Run Default value of EC Index 15h/16h/17h is 40h
Pin 27 & Pin 77	FAN_CTL_SEL	10 No Run Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run Default value of EC Index 15h/16h/17h is 00h
		00 75% Run Default value of EC Index 15h/16h/17h is 20h
JP5	WDT_EN	1 Disable WDT to rest PWROK
Pin 77	WDT_EN	0 Enable WDT to rest PWROK
JP6	SVID_EN	1 Disable SVID Function
Pin 60	SVID_EN	0 Enable SVID Function
JP7	Dual_BIOS_EN	1 Enable Dual BIOS Function for GigaByte Only
Pin 97	Dual_BIOS_EN	0 Disable Dual BIOS Function for GigaByte Only

IT8720CX-&gt;FX(and later) strapping change. JP1 no use, JP3 change to Low.

